

ABSTRACT OF THE DISCLOSURE

1 A semiconductor device including memory cells isolated by a trench that may be self
2 aligned with a stacked film pattern (7) has been disclosed. The memory cells may be flash
3 memory cells having an active gate film (2) that may be thinner than a gate oxide film (30).
4 The active gate film (2) may be located in a central portion under of a gate electrode (3). The
5 gate oxide film (30) may be located under end portions of the gate electrode (3). In this way,
6 a distance between a shoulder portion of a trench (11) and a gate electrode (3) may be
7 increased. Thus, an electric field concentration in the shoulder portion of the trench (11) may
8 be decreased and memory cell characteristics may be improved.

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